END TERM EXAMINATION

THIRD SEMESTER [B.TECH] DECEMBER-2024

Paper Code: ECC-207 ***Subject: Digital Logic & Computer Design***

Time: 3 Hours ***Maximum Marks: 60***

Note: Attempt five questions in all including Q. no.1 which is compulsory. Select one question from each unit.

Q1 Attempt all Questions

(a) Convert $(1111000100)_2$ to gray, XS-3 and BCD. **(4)**

(b) Implement half adder using NAND gate only. **(4)**

(c) What is race around condition in flip-flops? How can it is overcome? **(4)**

(d) Differentiate between Ring and Johnson counter. **(3)**

(e) What is an Input-Output processor (IOP), and how does it contribute to the efficiency of I/O operations? **(3)**

(f) Differentiate between RISC and CISC. **(2)**

UNIT-I

Q2 (a) Simplify the following boolean function using Quine-McCluskey Method. **(6)**

$f\{A,B,C,D\} = \square m\ (1, 2, 4, 5, 7, 8, 10, 11, 12, 14)$.

(b) Find a minimal SOP using K-Map and draw the circuit of minimal expression. **(4)**

$f\{A,B,C,D\} = \square m\ (1, 3, 4, 5, 9, 10, 11) + d\ (6,8)$.

Q3 (a) Design a 4-bit magnitude comparator circuit. Provide the truth table for the comparator. **(5)**

(b) Design a 16-to-1 multiplexer using 8-to-1 multiplexers. Provide the logic diagram and truth table for your design. **(5)**

UNIT-II

Q4 (a) Explain the concept of a modulus counter. Design a synchronous counter with a modulus of 9 using JK flip-flops. **(5)**

(b) How does a serial-in-parallel-out (SIPO) shift register differ from a parallel-in-serial-out (PISO) shift register? Consider a 4-bit serial-in, serial-out (SISO) shift register with an initial state of 1101. Assume a clock signal that triggers the shift operation on each rising edge. The input data is 1010. Illustrate the state transitions of the shift register for each clock cycle, showing the output after each shift operation. After four clock cycles, what will be the final state of the shift register? **(5)**

P.T.O.

Q5 (a) Design a sequence detector which detects 1100 (non overlapping) from any given sequence. Implement using D flip flop. **(5)**

(b) Describe the architecture of a Programmable Array Logic (PAL) device. How does it differ from a PLA in terms of structure and functionality? **(5)**

UNIT-III

Q6 (a) Explain the role of the control unit, ALU, and registers in the CPU. How do they work together to execute instructions? **(5)**

(b) Describe arithmetic micro-operations in the context of computer organization. Provide examples of arithmetic operations and how they are performed at the micro-operation level. **(5)**

Q7 (a) Define assembly language and describe its relationship with machine language. **(5)**

(b) Explain the concept of microprogrammed control in computer architecture. How does it differ from hardwired control, and what are its advantages? **(5)**

UNIT-IV

Q8 (a) Discuss the principles of cache mapping, including direct-mapped, set-associative, and fully associative cache mapping. **(5)**

(b) Describe the role of direct memory access (DMA) in input-output operations. **(5)**

Q9 (a) Define virtual memory. How does virtual memory address the limitations of physical memory? **(5)**

(b) Discuss the binary subtraction process and describe how borrow is handled in binary subtraction. **(5)**

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